CLAIMS

What is claimed:

1. A transistor device comprising:
   a source;
   a drain;
   a gate; and
   a metal channel.

2. The device of Claim 1 further comprising an insulating layer and a gate insulator, the metal channel being positioned between the gate insulator and the insulating layer.

3. The device of Claim 1 further comprising a silicon substrate.

4. The device of Claim 1 wherein the metal channel comprises a continuous thin conductive film having a thickness less than 5 nm.

5. The device of Claim 1 wherein the metal channel has a thickness in a range of 0.2 to 3 nm.

6. The device of Claim 1 wherein the transistor comprises an enhancement mode device.

7. The device of Claim 1 wherein the transistor comprises a depletion mode device.

8. A field effect transistor device comprising:
   a metal channel formed over an insulator;
   a source and a drain; and

a gate and a gate insulator formed over the channel.

9. The device of Claim 8 wherein the insulator further comprises an insulating layer over a substrate, the metal channel being positioned between the gate and the insulating layer and the gate insulator being positioned under the gate and over the metal channel.

10. The device of Claim 8 further comprising a silicon substrate.

11. The device of Claim 8 wherein the metal channel comprises a continuous thin conductive film having a thickness less than 5 nm.

12. The device of Claim 8 wherein the device further comprises a complementary transistor device.

13. The device of Claim 8 further comprising an encapsulation layer.

14. The device of Claim 8 wherein the metal channel has a length in a range of 5 nm to 50 nm and a width in a range of 50 nm to 500 nm.

15. The device of Claim 8 wherein the channel comprises a plurality of layers.